



VERIFICATION ACADEMY

Basic OVM

Constrained Random Verification Primer

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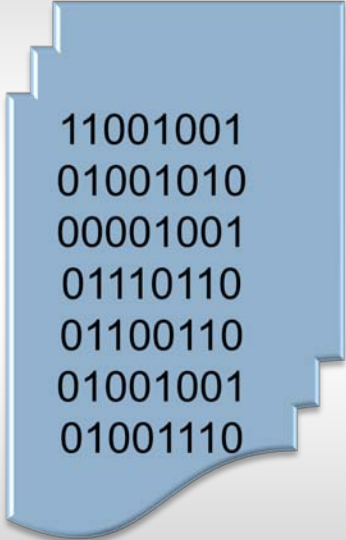


Sessions in this Module

1. **Constrained Random Verification Primer**
2. **Introduction to OVM**
3. **OVM "Hello World"**
4. **Connecting Env to DUT**
5. **Connecting Components**
6. **Introducing Transactions**
7. **Sequences and Tests**
8. **Monitors and Subscribers**



Stimulus



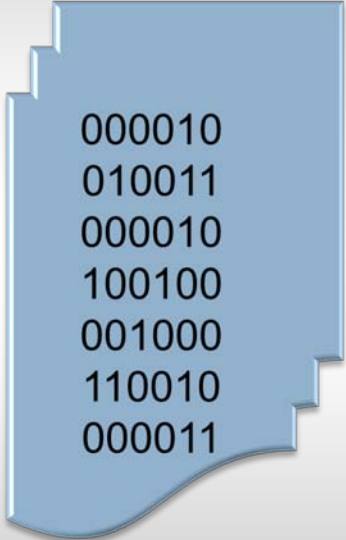
```
11001001
01001010
00001001
01110110
01100110
01001001
01001110
```



Design
Under
Test



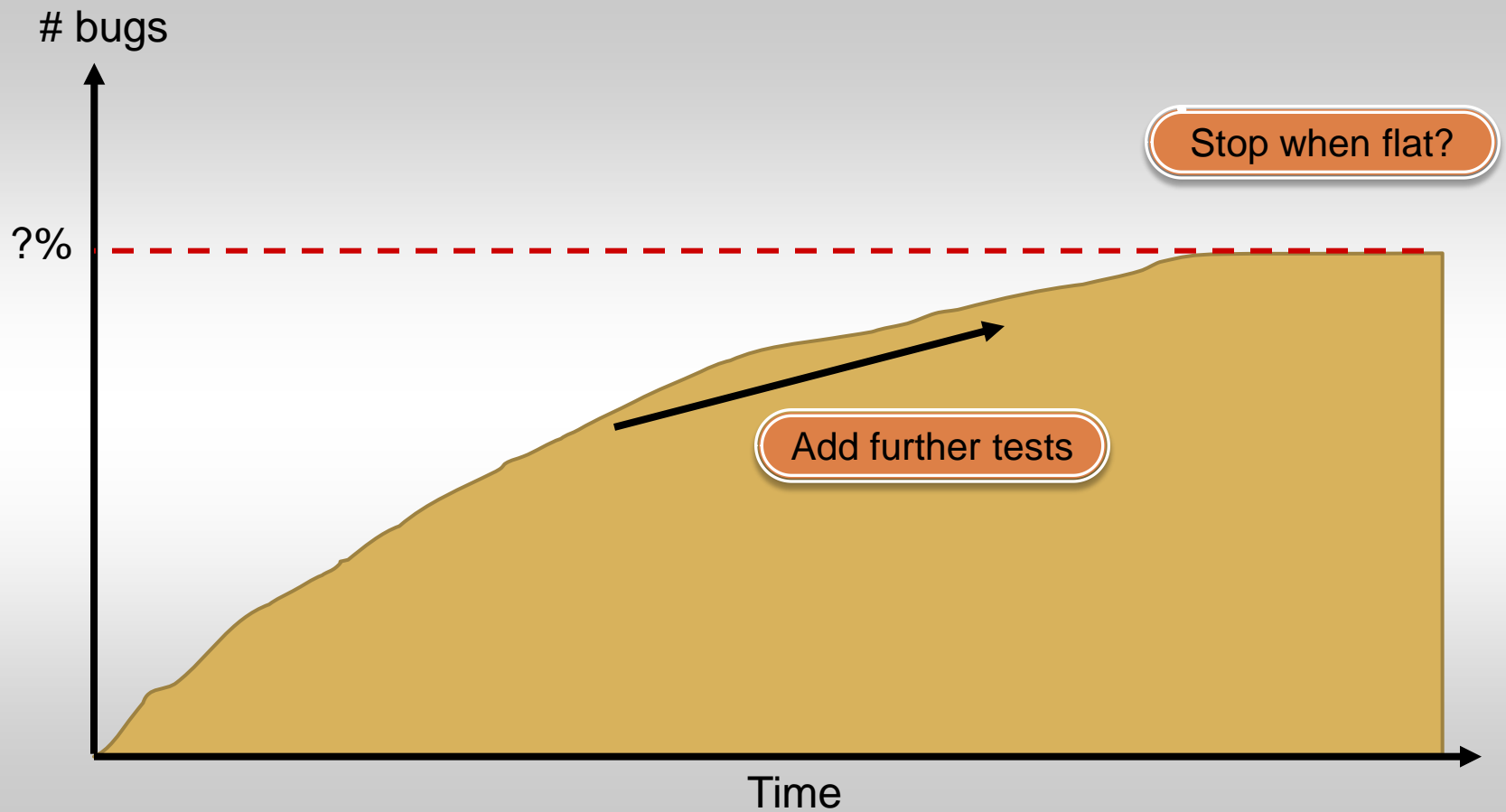
Results



```
000010
010011
000010
100100
001000
110010
000011
```

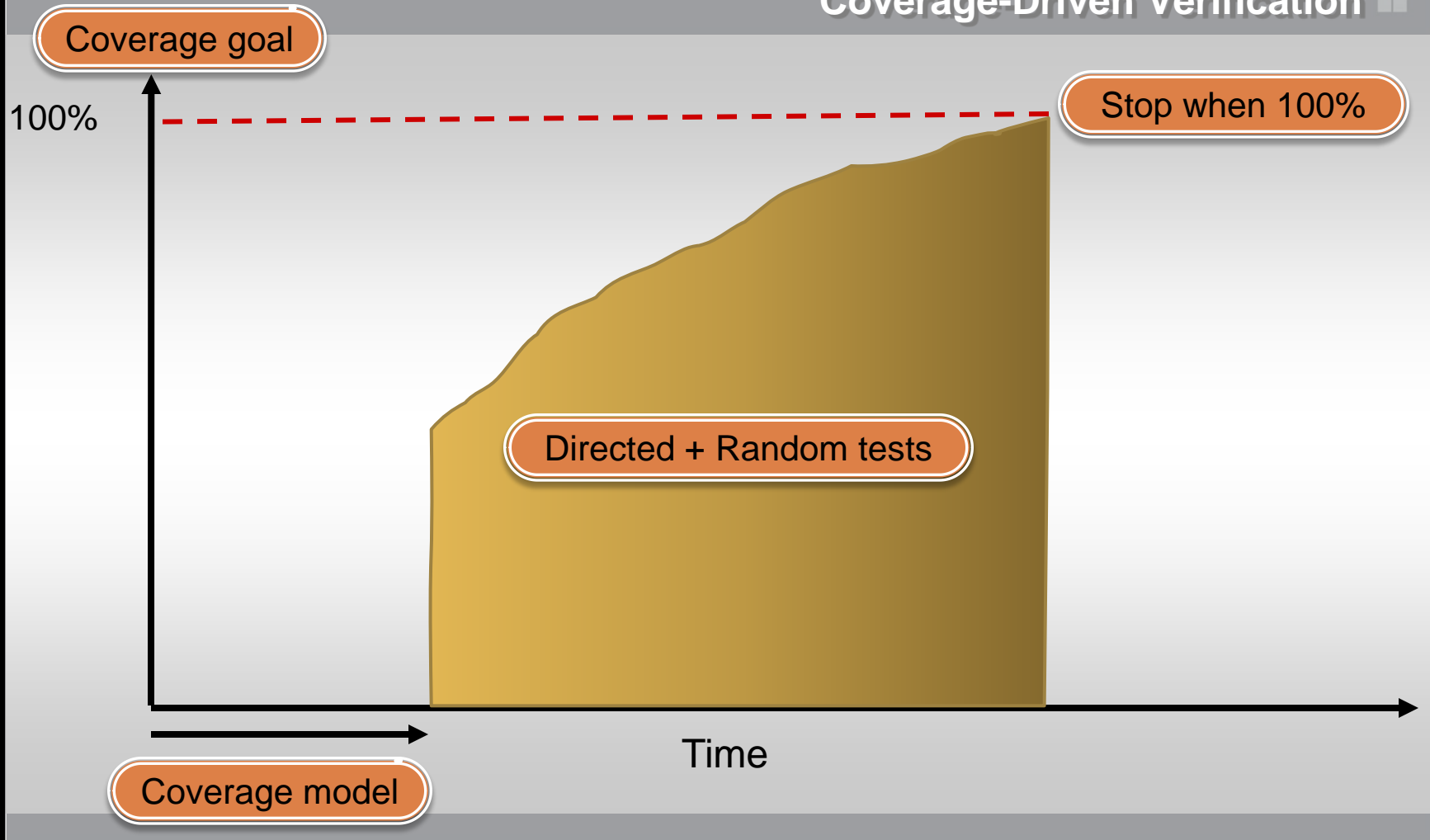


Simulation with Directed Tests



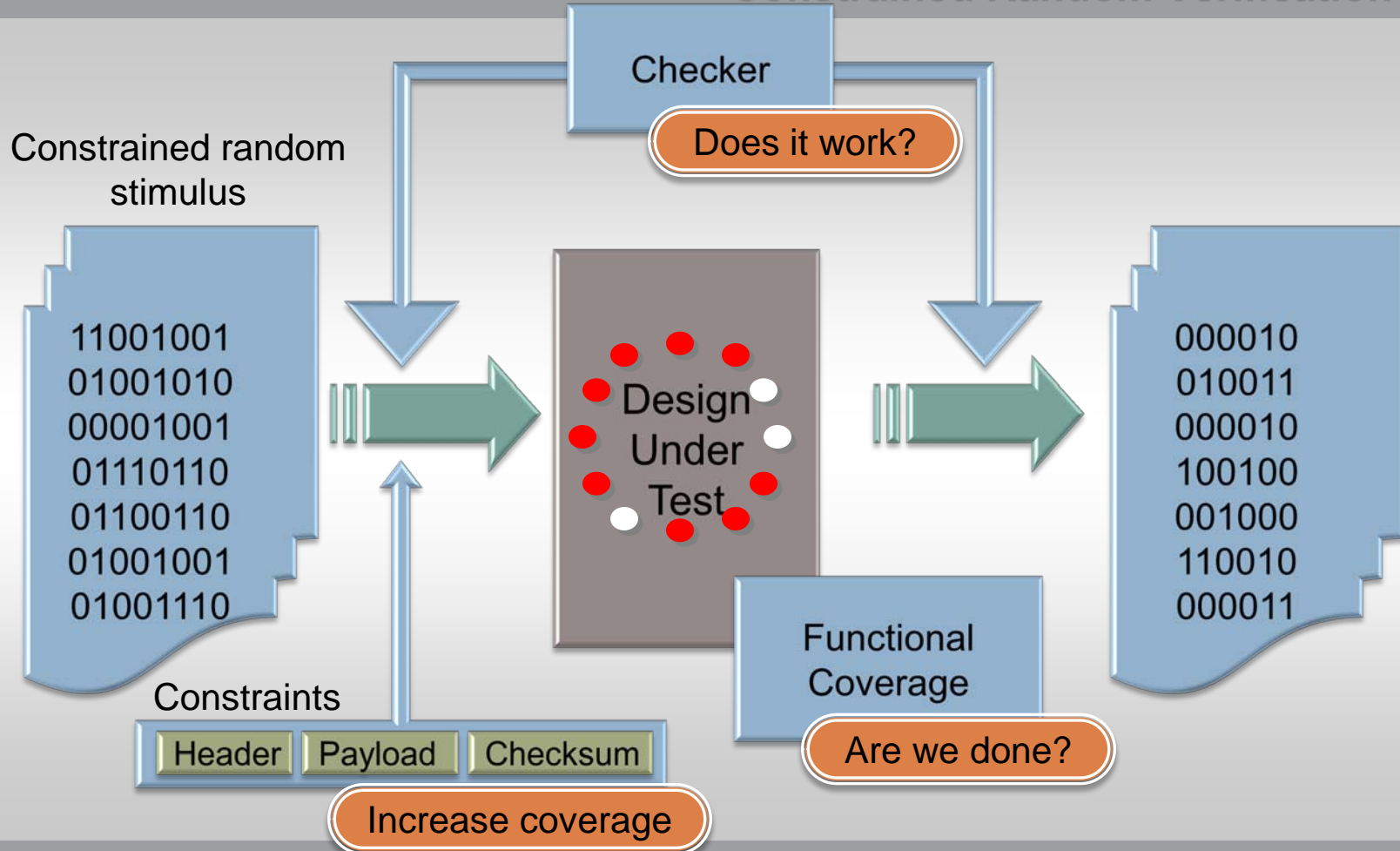


Coverage-Driven Verification





Constrained Random Verification





Test Planning

Test Plan

- The NBG output pin will reflect the status of the internal FAIL register bit
- A checksum calculated using the CCITT-16 polynomial is appended
- ...

Coverage Model

```
covergroup ...  
covergroup...  
covergroup...  
covergroup
```

```
cover ...  
cover ...
```

```
5: if (en)  
5:  q <= d;  
0: else
```

Tests

```
module test1;  
  random_seed = ...  
  verif_env(bus_if)  
  .....  
  ....  
  ...
```

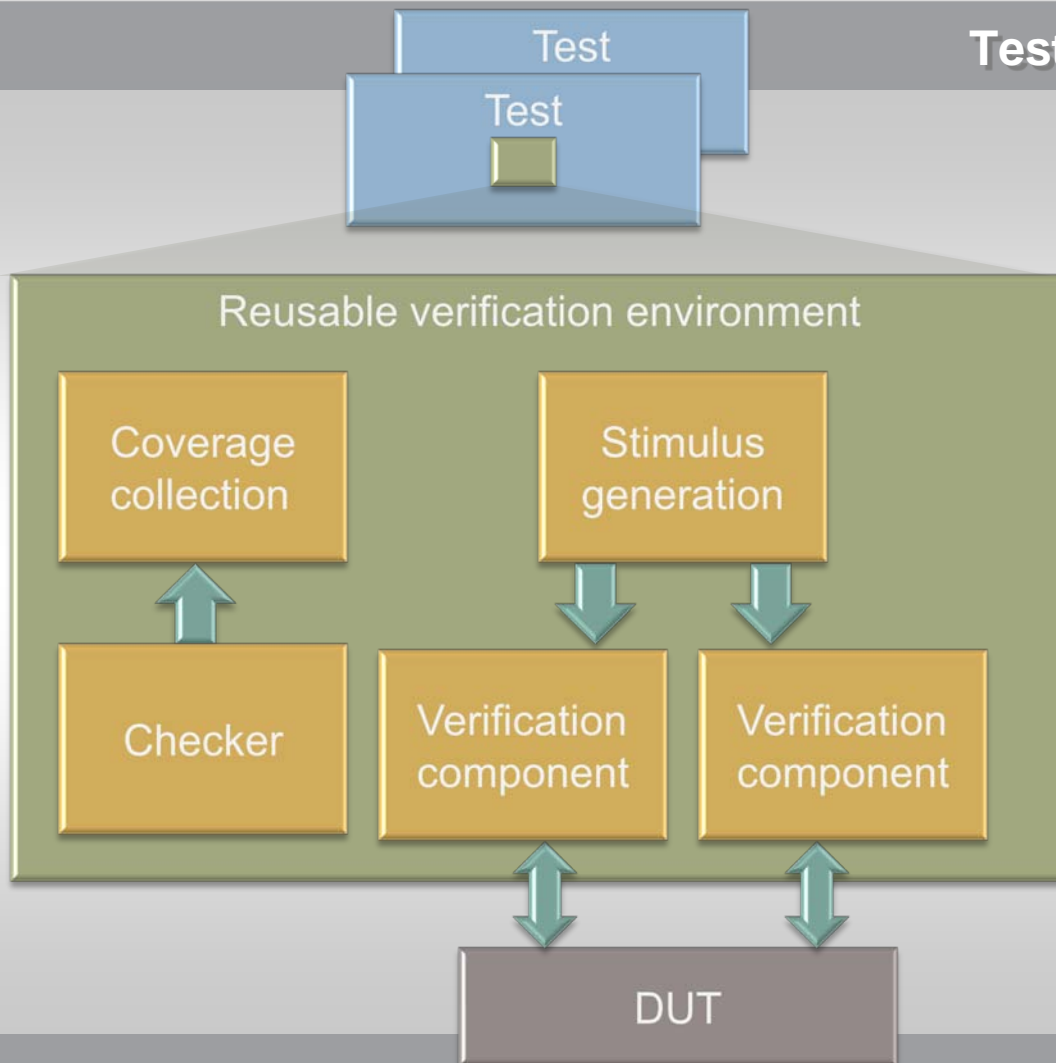
```
module test2;  
  constraint { ... }  
  verif_env(bus_if)  
  .....  
  ....
```

Back-annotate
coverage

Simulation

Grade tests

Iterate





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