Getting Started Using Mentor Graphic's ModelSim

There are two modes in which to compile designs in ModelSim, classic/traditional mode and project mode. This guide will give you a short tutorial in using classic/traditional mode. It is broken down into the following sections

- 1. Part 1: Compiling a Design
- 2. Part 2: Simulating a Design
- 3. Transitioning to the Next Lab
- 4. Setting Simulator Resolution
- 5. Directory Structures and Running Scripts

<u>1 Part 1: Compiling a Design</u>

1.1 Code Your Design

Code your design per the lab directions.

1.2 Start ModelSim

Start ModelSim by double clicking on the ModelSim Icon (windows) or by typing "vsim &" in the shell (UNIX). If you window does not look as below, select the menu command "Layout > Reset". Note the workspace, transcript and source windows can be moved.



1.3 Set the Working Directory

Use the ModelSim menu command "File > Change Directory" to set the working directory*. For lab 1, browse to the directory "VhdlIntro/Chipper/vhdl_src" as shown in the following dialog box.

Browse for Folder
Please choose a directory, then select OK.
C:\student\VhdlIntro\Chipper\vhdl_src
vhdl_src
WhdIntro Answers Chipper Sim_aldec Sim_mti Syn_synplicity VhdI_src DigitalClock
OK Cancel

Note if a simulation is active, you cannot run change directory. First you must end the simulation with the ModelSim menu pull down "Simulate > End Simulation".

1.4 Create a Work library

A library is a container of compiled VHDL designs. You can think of a library as a formal storage location for object files (similar to "C" language *.o files).

Before compiling your design, you must create the work library. Use the ModelSim menu command "File > New > Library" to create the work library. The library pop-up window should look like the following when you are done.

🗖 Create a New Lib 🔀
Create
🔘 a map to an existing library
 a new library and a logical mapping to it
Library Name:
work
Library Physical Name:
work
OK Cancel

1.5 Compile a Design

In order to run a simulation, all files (design and testbench) that are to be used in the simulation must be compiled. Use the ModelSim menu command "Compile > Compile" to compile a design (Inc.vhd for the first part of lab 1) into the work library. This causes the following pop-up window to appear. In the pop-up window select Inc.vhd and press the compile button.

Compile	Source Fi	iles			? ×
Library: wor	k	•			
Look in:	🔁 vhdl_src		•	⊨ 🗈 💣 🔳 ◄	
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My Network Places	File name: Files of type:	Inc.vhd HDL Files (*.v;*.vl;*	.vhd;*.vhdl;*.vho;*.ł	▼ ndl, [×] .vo; ▼	Compile Done
🔲 Compile selec	ted files together	Default Options.	Edit Sourd	ce	

After compiling your design successfully (check transcript window for error messages), close the pop-up dialog box by pressing "Done".

The key to understanding error messages is to realize that the message is produced after the compiler gets lost. In the example below (note this is not your lab design), the entity Adder8 has a ';' after the last port declaration. Most often this means that the error message will be generated on line 43. This is common, so make sure when you get an error message to read the specific error message and realize the root cause may be something done on the previous line that causes the compiler to "detect" the error on the current line.

```
39 -- Not the lab design
39 entity Adder8 is
40 port (
41 A, B : In std_logic_vector(7 downto 0);
42 Y : Out std_logic_vector(7 downto 0); -- error
43 );
44 end Adder8;
```

Also note that when you get an error message, you can double click on it and the ModelSim editor will take you to the line in error.

2 Part 2: Simulating a Design

2.1 Code the Testbench

Code the testbench per lab directions.

2.2 Compile the Testbench

Compile IncTb.vhd using the steps from "Compile a Design".

2.3 Load the Testbench = Start the Simulation

Go to the library tab of the workspace, press the plus sign to expand the work library, and right click on your testbench (inctb) and select simulate. Do not double click on your testbench as this starts an optimized simulation. Do not load your design (Inc), instead, it is loaded as a result of the testbench being loaded.

When the simulation loads, the simulation window will overlay the library window as shown below. You can switch back and forth between the two windows using the "sim" and "library" tabs. Close the Objects and Process windows by pressing on the "X" in the right corner.



2.4 Display Waveforms

Display the waveforms after loading the testbench and before running the simulation. To display waveforms, select the design under test (inc) in the "sim" tab, right-click the mouse, and select "Add > To Wave >All items in region".

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Alternately, bring up a wave window by selecting "View > Wave" in the ModelSim menu. Select a design (such as u_inc) in the "sim" tab of the ModelSim workspace and click and drag the design to the wave window.

2.5 Run the Simulation

For lab 1, you will be running your design for 720 ns. To do this, change the default run length (see picture above) to 720 ns (type it in the box). Now select "Simulate > Run > Run 100*". On some revisions, the 100 will be replaced by the actual run time.

Note that it is quite normal to see warning messages at the start of the simulation. Most messages that occur before a design is initialized and/or reset can be ignored. For example, the following warning results from the A input being initialized to "UUUUUUUUUUUUU" at time 0:

```
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic
operand, the result will be 'X'(es)!
# Time: 0 ns Iteration: 0 Instance: /inctb/u_inc
```

Note that if you forgot to display your waveforms before running the simulation or find a bug during simulation, you will need to re-run the simulation. See the next section for details.

2.6 Recompiling and Rerunning a Simulation

VHDL designs are required to be compiled bottom-up. If you find and fix a bug in your design, you will need to re-compile both the design (Inc.vhd) and the testbench (IncTb.vhd).

To re-run a simulation, instead of starting a simulation, use the restart command. Restarting a simulation sets the time to 0, reloads any recompiled designs, and maintains the current context (such as signals in the wave window). Restart a simulation by using ModelSim menu item "Simulate > Restart". This will cause the following pop-up to appear. Press the Restart button.



At this point you can set breakpoints, display additional signals, and run the simulation (using the Run command described previously).

2.7 Using the Waveform Window

All commands described in this section are done with the waveform window undocked. To undock the wave window press on the undock button (see diagram in the Displaying Waveforms section – it is the box with an arrow pointing out of it). The waveform window menus should now look as below (you may need to stretch it some). Other changes made to the wave window will be explained in this section. Note the same menu commands are available when the wave window is docked, however, they are more difficult to find.



2.7.1 Displaying Waveforms after Running a Simulation

If you display waveforms after running a simulation and want to see the waveforms from the beginning of time, you will need to restart your design (using the restart command) and rerun the simulation.

2.7.2 Zooming

When in the wave portion of the waveform window, pressing the right mouse button allows the following zoom options: In 2x, Out 2x, Full, Last, and Range. In addition, zooming to an area can be done by clicking the middle mouse button and then dragging in a horizontal direction.

2.7.3 Radix

The radix of the selected signal (or signals) can be specified using one of the following waveform menu commands.

Format > Radix > Hexadecimal
Format > Radix > Unsigned (positive decimal)
Format > Radix > Decimal (signed decimal)

Alternately you can access a similar menu with the right mouse button when selecting the signal(s).

2.7.4 Selecting Signals

Select one signal by clicking the left mouse button on its name.

To select multiple signals,

- 1. Select one signal and then press shift-left mouse button to select a range
- 2. Select one signal and then add more signals by pressing ctrl-left mouse button.

2.7.5 Moving Signals

Select signal(s) and drag to new location in wave window.

2.7.6 Using Cursors

The active cursor is shown in bold. To make a cursor the active cursor, click on it with the left mouse button. To add cursors, use the "Add > Cursor" waveform menu command. When more than one cursor is displayed, measurements can be made between adjacent cursors.

To accurately place a cursor, use the find next change symbols (shown below) to move the active cursor to the next change of the selected signal. Alternately dragging a cursor over an edge of the selected signal will cause the cursor to try to snap to the edge.

Find next change to right Find next change to left	\
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2.7.7 [Optional] Saving and Restoring Waveforms

To save waveforms, use the following waveform window menu:

File > Save Format . . .

To Load (Restore) waveforms, use the following waveform window menu:

File > Load Format . . .

2.7.8 [Optional] Selecting Individual Signals to Display

Add the objects window to the modelsim GUI using the menu command, "View > Objects". The window will now look as shown below. To display an individual signal in a given design, select the design in the sim window (such as u_inc shown), right click on a signal in the objects window and specify the "Add to Wave > Selected Signals". Note the new waveform for Z in the docked wave window.

ModelSim SE 10	0.0	
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Transcript VSIM 9>	IncTb.vhd	ave
Now: 1 us Delta: 1	sim:/inctb	0 ns to 107 ns

3 Transitioning to the Next Lab

There is no need to quit the simulator to go to the next lab. You can simply compile more designs into the library and then run another simulation.

Note that if the next lab is in a different directory that you need to end the simulation with the ModelSim menu command "Simulate > End Simulation", before you can use the change directory menu command "File > Change Directory".

4 [Optional] Setting Simulator Time Resolution

Simulator resolution is specified when loading a design for simulation. To set the simulator resolution, select "Simulate > Start Simulation" from the ModelSim menu. The resulting pop-up works just like the workspace library tab, except it also allows the simulation resolution to be specified as shown below.

Design VHDL Verilo	g] Libraries]	SDF Others		<u>الا الا</u>	
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	Entity Entity Optimized Optimized	C:/student/VhdlIntro/Chippe C:/student/VhdlIntro/Chippe I	r/vhdl_src r/vhdl_src		Use this as directed in lab 2 optional steps only.
Design Unit(s) work.inctb			Resolution		
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<u>5 Directory Structures & Running Scripts</u>

Currently we are running the simulator out of the VHDL source directory (vhdl_src). If you look in this directory, you will find that the simulator has added a few files to it (modelsim.ini, vsim.wlf, and the directory work). An alternate way to organize a project is to have a separate directory for source files and separate directories for the simulator and synthesis tools. The following directory structure is being used for these labs:



Exit out of the simulator. In the directory vhdl_src, delete any file that does not have a *.vhd extension. Delete the subdirectory work.

Start the simulator. Use "File > Change Directory" to go to the directory

VhdlIntro/Chipper/sim_mti. Execute the script (for Lab6 it is: **TbLedFlasher_lab6.tcl**) using "Tools > TCL > Execute Macro ...".