



VERIFICATION ACADEMY

Basic OVM

Introduction to OVM

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What is OVM?

- **The Open Verification Methodology**
- **Test benches for (System)Verilog / VHDL / SystemC designs**
- **SystemVerilog class library**
- **Open source (Apache licence)**
- **Backward compatible with AVM and URM**
- **Supports multi-language interoperability**



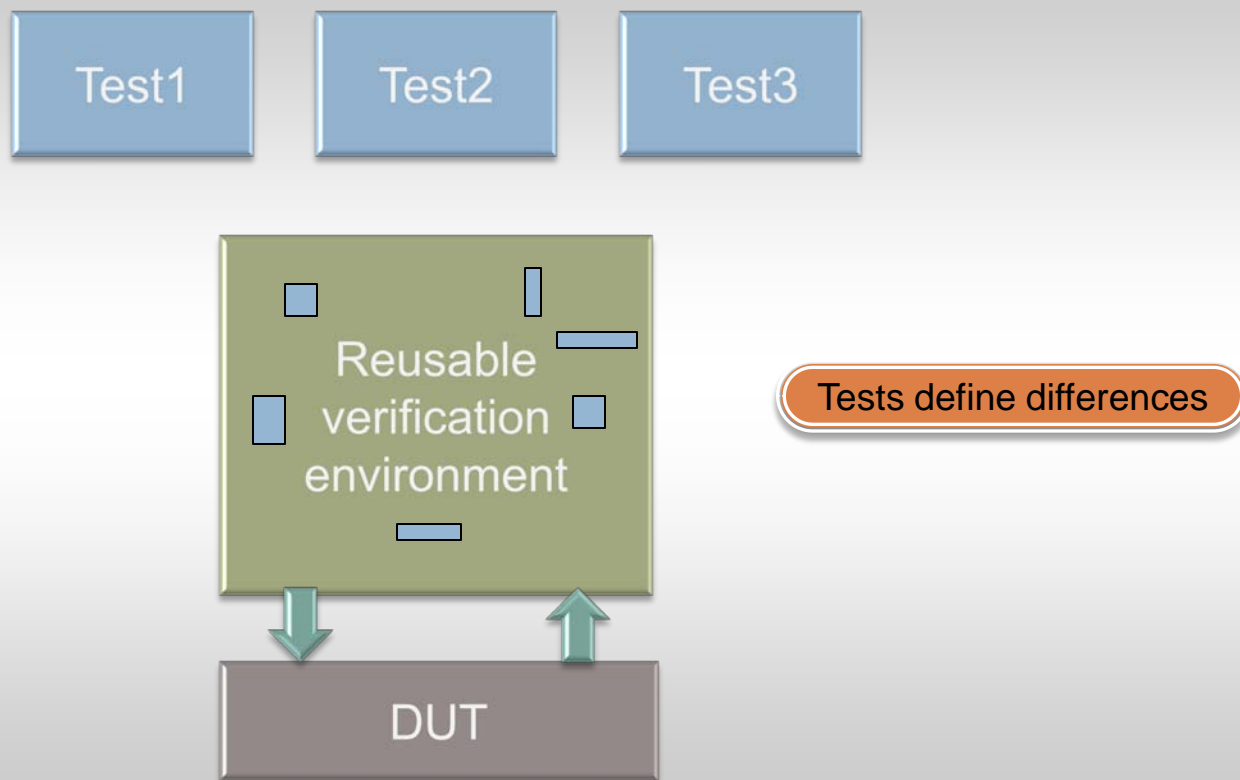
OVM Highlights

- **Constrained random, coverage-driven verification**
- **Configurable, flexible, test benches**
- **Verification IP reuse**

- **Separation of tests from test bench**
- **TLM communication**
- **Layered sequential stimulus**
- **Standardized messaging**



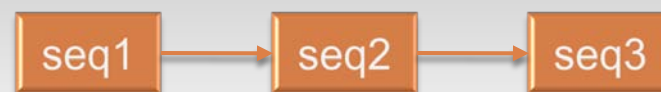
Test versus Testbench





Layered Sequential Stimulus

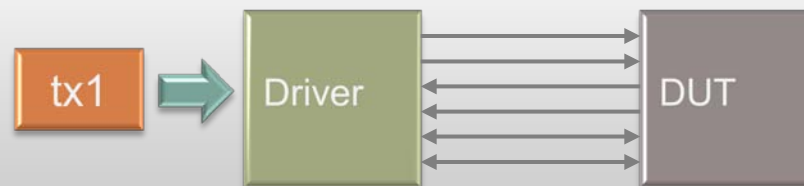
Nested, layered or virtual sequences



Constrained random sequence of transactions



Drive transactions into DUT





The Big Picture

Configure environment

Configuration table

name = value
name = value
name = value

Configure component

Reusable verification environment

Scoreboard

Virtual
sequencer

Monitor

Verification
component

Verification
component

DUT

Sequencer

Monitor

Driver



Open Verification Methodology

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Events

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QUICK LINKS

- ➔ [Mentor Graphics](#)
- ➔ [Cadence](#)
- ➔ [OVM Forum](#)
- ➔ [Community Contributions](#)

WHAT'S NEW

December 18, 2009

OVM 2.1 Release Now Available!
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OVM Cookbook
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Where's The "You" In The OVM?
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October 8, 2009

Updated VMM Kit for Questa and
Incisive Now Available for OVM
Interoperability
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OVM World

- ▶ Advanced Verification Capabilities
- ▶ Higher Levels of IP Integration
- ▶ Robust Class Library
- ▶ Open, Interoperable, Downloadable
- ▶ Supporting Multiple Languages and Simulators
- ▶ Extensive Technical Community Contributions



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Open Verification Methodology

Intro

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OVM Class Reference

The OVM Class Library provides the building blocks needed to quickly develop well-constructed and reusable verification components and test environments in SystemVerilog.

This OVM Class Reference Guide provides detailed reference information for each user-visible class in the OVM library. For additional information on using OVM, see the OVM User Guide located in the top level directory within the OVM kit.

We divide the OVM classes and utilities into categories pertaining to their role or function. A more detailed overview of each category-- and the classes comprising them-- can be found in the menu at left.

Base

This basic building blocks for all environments are components, which do the actual work, transactions, which convey information between components, and ports, which provide the interfaces used to convey transactions. The OVM's core *base* classes provide these building blocks. See [Core Base Classes](#) for more information.

Reporting

The *reporting* classes provide a facility for issuing reports (messages) with consistent formatting and configurable side effects, such as logging to a file or exiting simulation. Users can also filter out reports based on their verbosity, unique



What You Need to Learn

Verification Planning and Management

Constrained Random Verification

OVM Class Library (& OOP & TLM)

classes

SystemVerilog

assertions
coverage
constraints
interfaces



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